Name: Dr. Arindam Banerjee

Designation: Associate Professor

Branch: Electronics & Communication Engineering

Educational Qualification(s):

Qualification(s)	**University**
B.E.	Burdwan University
M.Tech	Maulana Abul Kalam Azad University of Technology (Formerly WBUT)
Ph.D in Engineering	Jadavpur University

Experience in years:

Academic: 13 Years

Details:

Sl. No.	Organization	Position Held	Duration	
			From	To
1	JIS College of Engineering	Assistant Professor (Associate Professor for last 05 months)	December, 2015	December, 2022
2	Jadavpur University	Research Associate	December, 2012	November, 2014
3	JIS College of Engineering	Assistant Professor (Associate Professor for last 05 months)	August, 2008	November, 2012

Industrial: 02 years

Details:

Sl. No.	Organization	Position Held	Duration	
			From	To
1	Tata Telephone Services	Maintenance Engineer	July, 2004	June, 2006

Other Information:

a) Publication details.

1. **A. Banerjee**, D. K. Das, “The design of reversible multiplier using ancient Indian mathematics”, ISED-2013, pages-31-35, December, 2013, Singapore.

2. **A. Banerjee**, D. K. Das, “Squaring in reversible logic using iterative structure”, East West Design and Test Symposium, 2014, Ukrain.

3.**A. Banerjee**, D. K. Das, “The Design of Reversible Signed Multiplier using Ancient Indian Mathematics”, Journal of Low Power Electronics, vol. 11, October, 2015, pp. 467-478. (SCI(M), Scopus I.F. – 0.84)

4. **A. Banerjee**, D. K. Das, “A New Squarer Design with Reduced Area and Delay”, IET Computers and Digital Techniques, vol. 10, issue 5, February, 2016, pp. 205-214. (SCI(E), I.F. – 0.515)

5. **A. Banerjee**, D. K. Das, “Squaring in Reversible Logic using Zero Garbage and Reduced Ancillary inputs”, Int. Symp. On VLSI Design, January, 2016.

6. **A. Banerjee**, D. K. Das, “Squarer Design with Reduced Area and Delay”, VLSI Design and Test Symp., May, 2015.

7. **A. Banerjee**, D. K. Das, “A New ALU Architecture Design using Reversible Logic”, Int. Symp. On Electronic Design (ISED-2016), December, 2016.

8. **A. Banerjee**, D. K. Das, “A Novel ALU Circuit based on Reversible Logic”, Journal of Circuits, Systems and Computers, World Scientific Publisher, Vol. 29, No. 11, 15th September, 2020. (SCI)

9. **Arindam Banerjee**, “Optimized Test Pattern Generation for Single Missing Gate Fault Detection in Reversible Arithmetic Circuits”, IEEE-EDKCON (International Conference)-2022, November, 2022 (Accepted and Presented).

10. **Arindam Banerjee**, Aniruddha Ghosh, Mainuck Das, SK Suman, Arvik Sai, “Memristor Based Multiplier and Squarer of some numbers of the form $10^l \pm m$”, Journal of The Institution of Engineers (India): Series B (IEIB), pp. 1239–1247, 2022 (published, DOI: 10.1007/s40031-022-00717-7).

11. **Arindam Banerjee** and Debesh Kumar Das, “Arithmetic Circuits Using Reversible Logic: A Survey Report”, Springer, LNCS. (Book chapter)

12. **A. Banerjee**, M. Das, A. Ghosh, “AI Based Online Data Segregation Method under COVID Situation”, IOCER-2020, 8-9 October, 2020 (published in IOP (Journal of Physics – Conference Series)

13.**A. Banerjee**, S. Bhattacharyya, A. Deyasi, “High Speed Reconfigurable ALU Design for Radix ($2^n \pm m$)”, Advances in Industrial Engineering and Management, American Scientific Publishers, vol. 5, no. 2, 2016, pp. 183-187, 2016. (ISSN: 2222-7059 (Print); E-ISSN: 2222-7067 (Online))

14. S. Pal, **A. Banerjee**, S. Bhattacharyya, “Optical Network Based RNS Multiplier in (2^n-1) Radix System using SOA-MZI”, NCRAST-2016 at Heritage Institute of Technology.

15. **A. Banerjee**, S. Pal, S. Bhattacharyya, D. K. Das, “Memristor Based Modulo Multiplier Design For (2^n-1) and 2^n Radix”, DevIC-2017, Kalyani Govt. Engineering College. (IEEE xplore)

16. **A. Banerjee**, S. Bhattacharyya, A. Deyasi, “Synthesis of High Speed Multi-valued ALU for (2^n±m) Radix”, MCCS-2017, Ranchi. (Springer, Book chapter)

17. **A. Banerjee**, S. Bhattacharyya, A. Deyasi, “Fast Squaring Technique for Radix Vicinity Numbers for Radix (2^n±m) with reduced Computational Complexity”, NCCS-2017, Ranchi. (Springer, Book chapter)

18. **A. Banerjee**, S. Pal, S. Bhattacharyya, D. K. Das, “Memristor Based MAC Architecture Design For (2^n-1) and 2^n Radix”, Journal of Active and Passive Electronic Devices, Old City Publishing, Philadelphia, Vol. 0, pp. 1-19, 2017 (SCI(M), ISSN: 1555-0281 (print), ISSN: 1555-029X (online)).

19. **A. Banerjee**, A. Ghosh, M. Das, SK Suman, A. Sain, “Memristor Based Fast Decimal Squaring of some numbers of the form 10^l±m”, FEMAS-2019, October, 2019 (Accepted and Presented).

20. Prabir Kumar Saha, **Arindam Banerjee**, Anup Dandapat, “High Speed Low Power Complex Multiplier Design Using Parallel Adders and Subtractors”, International Journal on Electronic and Electrical Engineering, (IJEEE),Vol 07,No. 11 Page No. 38-46, 2009.

21. Prabir Kumar Saha, **Arindam Banerjee** and A.Dandapat ,“Low power and High Speed Factorial Design in 22nm Technology”, accepted in AIP, 2010.

22. Prabir Saha, **A. Banerjee**, I. Banerjee and A. Dandapat, “High Speed Low Power Floating Point Multiplier Design Based on CSD (Canonical Sign Digit)”; Published in IJVED (National Journal).

23. P. Saha, **A. Banerjee**, A. Dandapat, P. Bhattacharyya, “Vedic Mathematics Based 32-Bit Multiplier Design for High Speed Low Power Processors”; Published in International Journal on Smart Sensing and Intelligent Systems.

24. Prabir Kumar Saha, **Arindam Banerjee**, A.Dandapat,P.Bhattacharyya, “ASIC design of a high speed low power circuit for factorial calculation using ancient Vedic mathematics”, accepted in Microelectronics Journal, Elsevier.

25. **A. Banerjee**, M. Das, A. Ghosh, “FPGA Implementation of High Speed Numerically Controlled Oscillator for QAM architecture”, accepted in National Conference NCACD to be held at HIT, Haldia, West Bengal, August, 2012.

26. **A. Banerjee**, R. Ghosh, S. Ghosh, “High Performance Novel Square root architecture using Ancient Indian Mathematics for High Speed Signal Processing”, accepted in National Conference NCACD to be held at HIT, Haldia, West Bengal, August, 2012.

27. Prabir Saha, **Arindam Banerjee**, Anup Dandapat and Partha Bhattacharya, "High Speed Vedic Multiplier for Decimal Number System"; VDAT-2012, Bengal Engineering and Science University, 2012.

28. **Arindam Banerjee**, Atin Mukherjee and Debesh Choudhury, "VHDL Implementation of Spatial Fourier Processing", ICONTOP-2012, Calcutta University, January, 2012.

29. **Arindam Banerjee**, Atin Mukherjee, Prabir K. Saha and Debesh Choudhury, "Computation of Fresnel Diffraction by VHDL", FOP-11, IIT-Delhi, December, 2011.

30. Prabir Saha, **Arindam Banerjee**, Partha Bhattacharyya, Anup Dandapat, "Vedic Divider: Novel Architecture (ASIC) for High Speed VLSI Applications"; ISED-2011, Kochi, 2011.

31. Prabir Saha, **Arindam Banerjee**, Partha Bhattacharyya, Anup Dandapat, "High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics"; Techsym-2011, IIT Kharagpur.

32. Prabir Saha, **A. Banerjee**, I. Banerjee and A. Dandapat, "High Speed Low Power Floating Point Multiplier Design Based on CSD (Canonical Sign Digit)"; IEEE symposium on VLSI Design and Testing (VDAT-2010), 2010.

33. Prabir Saha, Ranjana Roy, Ishita Banerjee, **Arindam Banerjee**, " FPGA Implementation of 2D convolution Architecture using Wave-front Array"; National Seminar on Recent Trends in Engineering and Technology Including Non-Conventional Energy,IMPS, Malda,April 10, 2010.

34. Prabir Kumar Saha, **Arindam Banerjee** and A.Dandapat, "Low power and High Speed Factorial Design in 22nm Technology", ICANN-2009, IIT Guwahati, December, 2009.

(b) Details of Seminar/Workshop/Conference.

1. **A. Banerjee**, D. K. Das, "The design of reversible multiplier using ancient Indian mathematics", ISED-2013, pages-31-35, December, 2013, Singapore.

2. **A. Banerjee**, D. K. Das, "Squaring in reversible logic using iterative structure", East West Design and Test Symposium, 2014, Ukrain.

3. **A. Banerjee**, D. K. Das, "Squaring in Reversible Logic using Zero Garbage and Reduced Ancillary inputs", Int. Symp. On VLSI Design, January, 2016.

4. **A. Banerjee**, D. K. Das, "Squarer Design with Reduced Area and Delay", VLSI Design and Test Symp., May, 2015.

5. **A. Banerjee**, D. K. Das, "A New ALU Architecture Design using Reversible Logic", Int. Symp. On Electronic Design (ISED-2016), December, 2016.

6. **Arindam Banerjee**, "Optimized Test Pattern Generation for Single Missing Gate Fault Detection in Reversible Arithmetic Circuits", IEEE-EDKCON (International Conference)-2022, November, 2022 (Accepted and Presented).

7. **Arindam Banerjee** and Debesh Kumar Das, “Arithmetic Circuits Using Reversible Logic: A Survey Report”, ACSS-2019, Kolkata, 2019.

8. **A. Banerjee**, M. Das, A. Ghosh, “AI Based Online Data Segregation Method under COVID Situation”, IOCER-2020, 8-9 October, 2020 (published in IOP (Journal of Physics – Conference Series)

9. **A. Banerjee**, S. Pal, S. Bhattacharyya, D. K. Das, “Memristor Based Modulo Multiplier Design For (2^n-1) and 2^n Radix”, DevIC-2017, Kalyani Govt. Engineering College.

10. **A. Banerjee**, S. Bhattacharyya, A. Deyasi, “Synthesis of High Speed Multi-valued ALU for (2^n±m) Radix”, MCCS-2017, Ranchi.

11. **A. Banerjee**, S. Bhattacharyya, A. Deyasi, “Fast Squaring Technique for Radix Vicinity Numbers for Radix (2^n±m) with reduced Computational Complexity”, NCCS-2017, Ranchi.

12. One Week Workshop on Digital Pedagogy, July, 2021, organized by JIS College of Engineering, Kalyani, Nadia, West Bengal.

13. One Week Workshop on Microchip AVR ATMEGA-16 Microcontroller Programming, August, 2021, organized by Microchip-Eduskills.